REMARKS

At the time the Official Action was mailed, claims 9-27 were pending in the present application. In the Official Action, the Examiner allowed claims 9 and 25-27, objected to claims 13, 14 and 16 and rejected claims 10-12, 15 and 17-24. Applicant thanks the Examiner for allowance of claims 9 and 25-27. Reconsideration of the remaining claims, as amended, is respectfully requested in view of the remarks set forth below.

Rejections under 35 U.S.C. § 112

The Examiner rejected claims 17 and 24 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to point out what is included and excluded in the claim language. Specifically, the Examiner rejected the use of the term, "approximately the same time," and asserted that this language made the claim an omnibus type claim. Applicant respectfully traverses these assertions.

It is well-settled that claims may properly recite relative language. The fact that claim language, including terms of degree, may not be precise, does not automatically render the claim indefinite under 35 U.S.C. § 112, second paragraph. *Seattle Box Co., v. Industrial Crating & Packing, Inc.*, 731 F.2d 818, 221 U.S.P.Q. 568 (Fed. Cir. 1984). Acceptability of the claim language depends on whether one of ordinary skill in the art would understand what is claimed, in light of the specification. M.P.E.P. § 2173.05(b).

Claim 17 recites "wherein the first latch is configured to produce the second output signal at approximately the same time as the second latch produces the fourth output signal." Claim 24 recites, "wherein each of the plurality of inter-domain test latches is configured to produce a respective output at approximately the same time when the test mode is enabled." As is clear from the present specification, the recited latches are enabled by the same signal

(TEST_CLK). However, as would be appreciated by those skilled in the art, the signal paths to each of the latches may vary in length. Accordingly, thought each latch is enabled by a common signal, the data may not be latched at exactly the same time, due to variations in signal path length and the like. Accordingly, the output is produced from each of the latches at *approximately* the same time.

Applicant respectfully submits that those skilled in the art would clearly understand the use of the relative term, in light of the present specification. Further, Applicant submits that the relative language does not classify the claim as an omnibus claim. Accordingly, Applicant respectfully requests withdrawal of the Examiner's rejection under 35 U.S.C. § 112, second paragraph.

Rejections under 35 U.S.C. § 102

The Examiner objected to claims 10-12, 15 and 18-24 under 35 U.S.C. § 102(b) as being anticipated by Ruparel (U.S. 5,689,517). Specifically, with regard to the independent claims, the Examiner stated:

> As per claim 10, Ruparel in (1b) teaches or discloses a circuit (see element 15) comprising a first clock domain (10a) comprising first edge triggered memory device (11a) for receiving first data input signal (see SCAN-IN input and clock signal CLK A) to produce first output signal and coupled to a first latch (12a) for outputting first output signal; second clock domain (10b) comprising a second edge triggered memory device (11b) for receiving a second input data and to produce third output signal (see line between 11b and 12b) coupled to a second latch (12b) for outputting forth output signal (see line L2).
>
> As per claim 18, Ruparel in figure (1b) teaches or discloses plurality of clock domains (see 10a-10c) coupled to each other through a test path (see the connections between the clock domains (SCAN-IN to SCAN-OUT) to receive a functional data and a clock signal (see SCAN-IN and CLK A and CLK B) wherein each of the clock domain comprises a test clock and a test data (see SCAN-IN and CLK A and CLK B)

> for producing an output data (SCAN-OUT). Although, Ruparel does not explicitly teach test selection input (multiplexer) for enabling test mode, this feature is deemed to be inherent to the system of Ruparel since Ruparel in column 2 lines 47-65 teach that most widely adopted scan technique is the mux-type-scan-D-flip-flop shown in figure 2a in which multiplexer (21) is used with D-flip-flop (22) and D-flip-flop (22) is typically a conventional D-flip-flop consisting of a master latch and a slave latch that operate together in response to a system clock and further the multiplexer (21) is connected to the input of D-flip-flop (22) to enable the mux-type-scannable-D-flip-flop (20) to select either Data-In input or Scan-In input by using a scan enable control signal (SE) (see col. 2, lines 47-65).

With regard to independent claim 10, while Applicant does not necessarily agree with the Examiner's rejections, claim 10 has been amended to include the subject matter previously recited in claim 13. Accordingly, claim 13 has been canceled. Based on the Examiner's indication of allowable subject matter, Applicant respectfully submits that this amendment is sufficient to place claim 10 in condition for allowance. Further, based on the Examiner's indication of allowable subject matter, claims 28-34 have been added to recite alternate combinations of allowable subject matter. Specifically, independent claim 28 recites the subject matter previously recited in claims 10 and 14. Applicant respectfully submits that new claims 28-34 are also in condition for allowance.

With regard to independent claim 18, Applicant respectfully traverses the Examiner's rejection. As recited in claim 18, each of the plurality of clock domains is configured to receive (1) a respective functional data signal (DATA) and (2) a respective clock signal (CLK 1-CLK 3). Claim 18 further recites that each of the plurality of clock domains comprises (1) a test clock input placing the test clock (TEST_CLK), (2) a test data input for receiving test data (SDI), (3) a test data output for producing output data (SDO) and (4) a test selection input for enabling a test mode (ST). For the Examiner's convenience, Applicant has included

the corresponding signal names in parentheses to provide a better understanding of the recited subject matter.

The Examiner correlated various features disclosed in Fig. 1b of the Ruparel reference with the above-referenced recited elements. The following chart provides a comparison of the presently recited elements and the features asserted by the Examiner to correlate with those features:

Recited Elements	**Asserted Feature**
DATA	SCAN-IN
CLK 1-CLK3	CLK A and CLK B
TEST_CLK	CLK A and CLK B
SDI	SCAN-IN
SDO	SCAN-OUT
SCAN TEST	*

As indicated above, the Examiner twice asserted the same features for two of the recited elements. For instance, the Examiner correlated each of the recited data signal (DATA) and recited test data input (SDI) with the SCAN-IN input of Ruparel. Further, the Examiner correlated each of the recited respective clock signal (CLK 1-CLK3) and the recited test clock input (TEST_CLK) with the CLK A and CLK B disclosed in Ruparel. Applicants respectfully assert that this duplication of corresponding features demonstrates that the Ruparel reference does not disclose each of the features recited in claim 18. By comparing Fig. 3 of the present reference, illustrating the recited elements, with Fig. 1b of the Ruparel reference, the errors in the Examiner's assertions becomes clear. For instance, each

of the plurality of clock domains in the Ruparel reference *does not* receive a common test clock input (TEST_CLK), as indicated in Fig. 3 and recited in claim 18. Accordingly, it is clear that the Ruparel reference does not disclose a plurality of clock domains comprising "a test clock input for receiving a test clock," as recited in claim 18. For at least this reason, the Ruparel reference cannot possibly anticipate the recited subject matter.

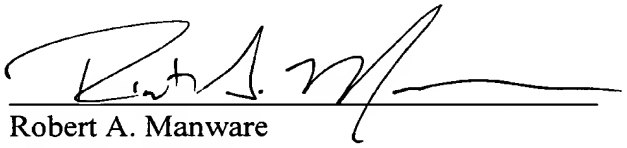
Further, the Examiner indicated that the test selection input for enabling a test mode is not taught by Ruparel, but further asserted that this feature is inherent in the system of Ruparel. While Applicant does not necessarily agree with this assertion, the point is moot since the Ruparel reference does not disclose each of the features recited in claim 18. Accordingly, Applicant respectfully requests withdrawal of the Examiner's rejection and allowance of claim 18, as well as those claims dependent thereon.

Conclusion

In view of the remarks and amendments set forth above, Applicant thanks the Examiner for allowance of claims 9 and 25-27. Further, Applicant respectfully requests allowance of claims 10-12 and 14-34. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: June 21, 2004



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